AMENDMENT

In the Claims:

Please substitute Claims 1, 5, and 10 presented below in marked-up form for previous Claims 1, 5, and 10. A complete listing of all claims is as follows.

1. (**currently amended**) A method of making a MOSFET, comprising:

first providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

second performing a source/drain extension implant;

third forming a spacer on the gate;

fourth performing epitaxy to form raised source/drain regions;

fifth forming a silicide on the gate and source/drain regions;

sixth removing the spacer, thereby forming a void region between the source/drain regions and the gate;

seventh performing a halo implant through the void, thereby forming a halo around the gate in the channel region; and

eighth completing the MOSFET.

2. (**original**) A method as recited in claim 1, wherein the source/drain extension implant comprises an approximately vertical implant to a depth of approximately 10 nm to 30 nm of ions selected from the group consisting essentially of B^+, BF_2^+, As^+, Sb^+, P^+.

3. (**original**) A method as recited in claim 1, wherein the spacer comprises a nitride.

4. (**original**) A method as recited in claim 1 wherein the halo implantation comprises an approximately vertical implant to a depth of approximately 40 nm to 100 nm of ions selected from the group consisting essentially of B^+, BF_2^+, Ga^+, In^+, As^+, Sb^+, P^+.

5. (**currently amended**) A method of making a MOSFET, comprising:

first providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

second performing a vertical source/drain extension implant to a depth of approximately 10 nm to approximately 30 nm;

thereafter, forming a spacer on the gate;

forming raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer, thereby forming a void region through the silicide between the source/drain regions and the gate;

performing a halo implant through the void, thereby forming a halo around the gate in the channel region; and

completing the MOSFET.

7. (**cancelled**)

6. (**original**) A method as recited in claim 5, wherein the spacer comprises a nitride.

8. (**original**) A method as recited in claim 5, wherein the source/drain regions are formed by epitaxy.

9. (**original**) A method as recited in claim 5 wherein the halo implantation comprises an approximately vertical implant to a depth of approximately 40 nm to 100 nm of ions selected from the group consisting essentially of B^+, BF_2^+, Ga^+, In^+, As^+, Sb^+, P^+.

10. (**currently amended**) A method of making a MOSFET, comprising:

providing a substrate having an isolation trench and a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

performing an approximately vertical source/drain extension implant in a region from the isolation trench to the gate, to a depth of approximately 10 nm to approximately 30 nm;

forming a nitride spacer on the gate;

performing epitaxy to form raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer, thereby forming a void region through the silicide between the source/drain regions and the gate;

performing an approximately vertical halo implant to a depth of approximately 40 nm to approximately 100 nm, thereby forming a void region around the gate in the channel region; and

completing the MOSFET.

11. (**original**) A method as recited in claim 10 wherein the halo implantation comprises implantation of ions selected from the group consisting essentially of B^+, BF_2^+, Ga^+, In^+, As^+, Sb^+, P^+.